REMARKS

Claims 1, 3-4, 6, 15-22 and 24-38 are presented for further examination without amendment.

In the Office Action mailed May 17, 2004, the Examiner rejected claims 1, 3-4, 6, 15-22, and 24-38 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,336,158 ("Martwick") in view of IEEE "Transactions On Very Large Scale Integration (VLSI) Systems," Vol. 7, No. 2, June 1999, Pages 212-221 ("Ramprasad").

Applicants respectfully disagree with the basis rejection and request reconsideration and further examination of the claims.

As discussed in the specification of the above-referenced application, the present invention is directed to encoder/decoder architecture and a related processing system that enables configuring the system in one from among three configurations to optimize performance in terms of timing, i.e., the delay in the critical path is minimized to reduce the latency of the bus accesses (see specification, page 8, lines 12-14). This is accomplished by providing at least one memory element for storing respective preceding input information and output information values, a prediction block for generating an estimate of the current input information value on the basis of the preceding input information value, and a decorrelation block for decorrelating the current input information value with respect to the estimate and to produce a decorrelation result adapted to be selected from one of the following: the current input information value, the preceding output value, or the decorrelation result. The present invention also includes a redundant line configured to transfer information on the sequentiality of the information, acting as a prediction block, an Xor logic gate acting as a decorrelation block, and a multiplexor acting as a selection block for selecting the current output value. These functional limitations are configured into these components to achieve the purposes of the present invention.

Martwick, U.S. Patent No. 6,336,158 is directed to memory-based I/O decode arrangement, system, and method of using the same. Martwick is specifically directed to interfacing a PCI bus with one or more busses of a different standard, such as an ISA bus. As shown in Martwick's Figure 1 a PCI bus 102 and ISA bus 103 are coupled via a bus bridge 108 in the form of an I/O controller 108. Martwick teaches in Figure 2 a process for executing a bus

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transaction between these dissimilar bus configurations wherein positive decode agents are given the opportunity to determine ownership of the transaction, and in the absence thereof, the controller 108 determines first if its map indicates the transaction is owned by the controller, and if not, a subtractive decode agent may then claim the transaction in step 208. (This is described at column 6, lines 1-30 of Martwick).

Martwick teaches at column 6, line 52-column 9, line 43 in greater detail the process for decoding transaction address signals to determine which agent will own the transaction. Nowhere does Martwick teach or suggest the use of a prediction block, a decorrelation block, and at least one register for selecting one from among current input information value, a decorrelation result, and a preceding output value. Moreover, as the Examiner acknowledges, Martwick does not disclose or suggest the use of a redundant line. For this, the Examiner refers to the teachings of Ramprasad.

Ramprasad teaches an architecture adapted to be used as a model for generating different encoding schemes, that is, in practice, to design different circuits adapted to be embodied separately, each circuit being adapted to be implemented as a single, respective encoding scheme. This is contrary to the present invention, which is configured to select one from among current information values, preceding output values, and a decorrelation result. Thus, Ramprasad teaches that once embodied in a certain circuit at the microelectronic level, such an encoding scheme is fixed and can no longer be modified. Also, at least some of the encoding schemes taught by Ramprasad are characterized by quite significant critical paths. See, for instance, the 700-800 gates referred to in connection with the pbm and vbm functions.

In contrast, the present invention relates to a universal architecture adapted to be implemented as such and includes the three blocks P, D, and S. These blocks can be specialized (either during the final steps of manufacture or even during run time while the system is operating, in order to implement a specific encoding scheme as desired). Specifically, the output block is configured in such a way that the output value can be selected to correspond to i) the present input value, ii) the preceding output value, or iii) the decorrelation of the current input value and the predicted value thereof. In addition to providing this degree of universality, the invention also minimizes the delay in the critical path, thus reducing the latency of the bus

accesses. This solution, *i.e.*, the provision of an output block configured in such a way that the output value can be selected to correspond to i) the present input value, ii) the preceding output value, or iii) the decorrelation of the current input value and the predicted value thereof is not disclosed or suggested by Ramprasad.

While the Examiner asserts that the combination of Martwick and Ramprasad obviates the present claimed invention, applicants respectfully disagree. The disclosure of Martwick, while showing the use of a few common discrete components, does not teach or suggest the configuration of these components in such a way to accomplish the claimed invention. The combination of the teachings of Ramprasad with Martwick fails to elevate Martwick to the configuration and functionality of the present claimed invention.

More particularly, while Martwick teaches the use of certain logic gates for parsing address signals to determine if a signal is claiming ownership of a particular transaction, nowhere does Martwick teach or suggest using at least one memory element for storing respective preceding input information values and output information values, a prediction block for generating an estimate of the current input information value on the basis of the preceding input information value, and a decorrelation block for decorrelating the current input information value with respect to the estimate, to produce a decorrelation result, the current output value adapted to be selected as one of the following: i) the current input information value, ii) the preceding output value, and iii) the decorrelation result. Moreover, nowhere do Martwick or Ramprasad, taken alone or in any combination thereof, teach or suggest the further recitation of claim 1 wherein a redundant line is preferably configured to transfer information on the sequentiality of the information and acting as a prediction block, an Xor logic gate acting as a decorrelation block and a multiplexor acting as a selection block for selecting the current output value in accordance with the previously recited elements of claim 1. Rather, the combination of Ramprasad and Martwick would merely add a redundant line to the address parsing scheme of Martwick, which would fail to enhance its functionality much less achieve the claimed combination of the present invention as recited in claim 1.

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Hence, applicants respectfully submit that claim 1, and all claims depending therefrom, as well as independent claims 15, 22, and 24-38 are also allowable for the foregoing reasons.

In the event the Examiner disagrees or finds minor informalities that can be resolved by telephone conference, the applicants respectfully request a telephone conference with the Examiner to expeditiously resolve prosecution of this application. Applicants' undersigned representative can be reached at (206) 622-4900.

Accordingly, applicants respectfully submit all of the claims in this application are now in condition for allowance. Early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

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